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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/691,078	10/21/2003	Qiang Shen	38571-2	9309

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EXAMINER	
GANDHI, DIPAKKUMAR B	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 09/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/691,078	SHEN, QIANG	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2004* & 10/21/2003. AR

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) *10-25,34 and 35* is/are withdrawn from consideration by Pre-Amendment. AR

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 26-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/13/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 3, 8, 33 are rejected under 35 U.S.C. 102(e) as being anticipated by Yano et al. (US 6,526,539 B1).

Yano et al. anticipate claim 1.

Yano et al. teach a method for decoding input data, said method comprising: (a) inputting a first set of symbols and a second set of symbols; (b) decoding the first set of symbols and a feedback set of symbols using a decoder, thereby obtaining a first set of decoded symbols; (c) interleaving the first set of decoded symbols, thereby obtaining a first set of interleaved symbols; (d) decoding the first set of interleaved symbols and the second set of symbols using the decoder, thereby obtaining a second set of decoded symbols; (e) de-interleaving the second set of decoded symbols, thereby obtaining a second set of de-interleaved symbols; and (f) repeating steps (b) through (e) for at least one additional iteration, wherein at each iteration the feedback set of symbols is the second set of de-interleaved symbols obtained during the immediately previous iteration (figure 5, col. 6, lines 47-52, col. 11, lines 48-65, col. 12, lines 53-61, Yano et al.).

- Yano et al. anticipate claim 2.

Yano et al. teach a method, wherein identical hardware is used for decoding in step (b) as for decoding in step (d), (col. 6, lines 35-39, Yano et al.).

- Yano et al. anticipate claim 3.

Yano et al. teach a method, wherein the decoder is an a posteriori probability decoder (col. 15, lines 58-61, Yano et al.).

- Yano et al. anticipate claim 8.

Yano et al. teach a method, wherein steps (b) through (e) are repeated for a predetermined number of iterations (col. 6, lines 47-52, Yano et al.).

- Yano et al. anticipate claim 33.

Yano et al. teach an apparatus for decoding input data, said apparatus comprising: (a) means for inputting a first set of symbols and a second set of symbols; (b) means for decoding the first set of symbols and a feedback set of symbols using a decoder, thereby obtaining a first set of decoded symbols; (c) means for interleaving the first set of decoded symbols, thereby obtaining a first set of interleaved symbols; (d) means for decoding the first set of interleaved symbols and the second set of symbols using the decoder, thereby obtaining a second set of decoded symbols; (e) means for de-interleaving the second set of decoded symbols, thereby obtaining a second set of de-interleaved symbols; and (f) means for repeating the functionality of means (b) through (e) for at least one additional iteration, wherein at each iteration the feedback set of symbols is the second set of de-interleaved symbols obtained during the immediately previous iteration (figure 5, col. 6, lines 47-52, col. 11, lines 48-65, col. 12, lines 53-61, Yano et al.).

3. Claims 26, 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Keevill et al. (US 6,359,938 B1).

Keevill et al. anticipate claim 26.

Keevill et al. teach an apparatus for decoding input data, said apparatus comprising: input means for inputting coded data (figure 15, col. 36, lines 62-63, Keevill et al.); buffering means for inputting, storing and outputting data (buffer 254 in figure 23, col. 22, lines 21-23, Keevill et al.); first register means for storing a portion of the data output from said buffering means (col. 7, lines 59-61, Keevill et al.); first read/write means for controlling writing of the data into said first register means and reading of the data out of said first register means so as to change the order of the data (col. 36, lines 27-32, Keevill et al.); decoding means for decoding a combination of at least part of the coded data provided by said input

means and the data read out of said first register means (figure 15, col. 7, lines 43-46, Keevill et al.); second register means for storing data output by said decoding means (col. 7, lines 59-61, Keevill et al.); second read/write means for controlling writing of the data into said second register means and reading of the data out of said second register means so as to change the order of the data, wherein the data read out of said second register means is stored in said buffering means (col. 36, lines 27-32, Keevill et al.);; third register means coupled to said buffering means (col. 7, lines 59-61, Keevill et al.); and third read/write means for transferring the data out of a portion of said buffering means into said third register means and then transferring the same data from said third register means back into said portion of said buffering means, but in a different order, and for then repeating said transferring steps for different portions of said buffering means (col. 36, lines 27-32, Keevill et al.).

- Keevill et al. anticipate claim 32.

Keevill et al. teach an apparatus, wherein said first register means, said second register means, and said third register means are capable of storing only a fraction of the data that said buffering means is capable of storing (col. 7, lines 59-61, col. 27, line 16, Keevill et al.).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yano et al. (US 6,526,539 B1) as applied to claim 1 above, and further in view of Shibutani et al. (US 6,631,491 B1).

As per claim 4, Yano et al. substantially teach the claimed invention described in claim 1 (as rejected above).

However Yano et al. do not explicitly teach the specific use of a method, wherein interleaving in step (c) comprises: (c1) writing the first set of decoded symbols into a buffer, row-by-row; (c2) reading from the buffer and writing into a row register a row of the first set of decoded symbols; (c3) reading from the row register and writing into the buffer the row of the first set of decoded symbols, so as to perform column interleaving; (c4) reading from the buffer and writing into a column register a column of the first set of decoded symbols; and (c5) reading from the column register the column of the first set of decoded symbols, wherein steps (c4) and (c5) together result in row interleaving.

Shibutani et al. in an analogous art teach an interleaving method for inputting a data series of a unit length and outputting an interleaved data series of the unit length, characterized by: a first step of writing said data series to a first interleaver in one direction; a second step of reading out column data or row data from said first interleaver, writing said read out data to a second interleaver, which has a size different from a size of said first interleaver, in one direction, and repeating said reading out column data or row data and said writing read out data column by column or row by row; a third step of reading out data column by column or row by row from each of interleavers generated by said second step, and writing said data to an interleaver which has a size the same as the size of said first interleaver, and reading out data from said interleaver generated by said third step, and outputting said interleaved data series (col. 29, lines 13-32, Shibutani et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yano et al.'s patent with the teachings of Shibutani et al. by including an additional step of using a method, wherein interleaving in step (c) comprises: (c1) writing the first set of decoded symbols into a buffer, row-by-row; (c2) reading from the buffer and writing into a row register a row of the first set of decoded symbols; (c3) reading from the row register and writing into the buffer the row of the first set of decoded symbols, so as to perform column interleaving; (c4) reading from the buffer and writing into a

column register a column of the first set of decoded symbols; and (c5) reading from the column register the column of the first set of decoded symbols, wherein steps (c4) and (c5) together result in row interleaving.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to improve error correction ability of an error correction code for burst error.

- As per claim 5, Yano et al. and Shibutani et al. teach the additional limitations.

Shibutani et al. teach a method according to claim 4, wherein de-interleaving in step (e) comprises: (e1) writing into a second column register the column of the second set of decoded symbols; (e2) reading from the second column register and writing into the buffer the column of the second set of decoded symbols, wherein steps (e1) and (e2) together result in row interleaving; (e3) reading from the buffer and writing into the row register the row of the second set of decoded symbols; and (e4) reading from the row register and writing into the buffer the row of the second set of decoded symbols, so as to perform column interleaving (figure 50, col. 27, lines 47-65, col. 29, lines 13-32, Shibutani et al.).

- As per claim 6, Yano et al. and Shibutani et al. teach the additional limitations.

Shibutani et al. teach a method, wherein step (c4) is performed prior to step (e2) for each column in the buffer (col. 29, lines 13-32, Shibutani et al.).

- As per claim 7, Yano et al. and Shibutani et al. teach the additional limitations.

Shibutani et al. teach a method according to claim 1, wherein a single buffer is used for both interleaving in step (c) and de-interleaving in step (e), (figure 5, col. 11, lines 16-26, Shibutani et al.).

7. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yano et al. (US 6,526,539 B1) as applied to claim 8 above, and further in view of Wang (US 6,014,411).

As per claim 9, Yano et al. substantially teach the claimed invention described in claim 8 (as rejected above).

However Yano et al. do not explicitly teach the specific use of a method, further comprising a step of making a hard decision for each bit position of said input data after completion of said predetermined number of iterations.

Wang in an analogous art teaches that at the end of each iteration, a hard decision is made on each bit based on the data bit estimates. The final decoded bit is declared to be a one if the majority of the hard decisions on this particular bit from all previous iterations is one, and otherwise is declared to be zero (col. 14, lines 48-52, Wang).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yano et al.'s patent with the teachings of Wang by including an additional step of using a method, further comprising a step of making a hard decision for each bit position of said input data after completion of said predetermined number of iterations.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to accurately determine the output data bits using the majority of values of the data bits.

8. Claims 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keevill et al. (US 6,359,938 B1) as applied to claim 26 above, and further in view of Penzel (US 4,394,753).

As per claim 27, Keevill et al. substantially teach the claimed invention described in claim 26 (as rejected above).

However Keevill et al. do not explicitly teach the specific use of an apparatus, wherein data positions in said buffering means are conceptually arranged in columns of data positions and rows of data positions, wherein said first register means and said second register means are for storing a column of data, and wherein said third register means is for storing a row of data.

Penzel in an analogous art teaches the present invention relates to a memory module, and more particularly to an integrated memory module having memory cells arranged in a matrix and addressable by row and column addresses, in which a plurality of address input terminals are provided for receiving the address signals, an address buffer memory is connected to the input terminals for receiving an address with a row address decoder and a column address decoder for forming row and column selection signals, and in which a data input and a data output are provided (col. 1, lines 8-18, Penzel). Penzel also teaches a memory medium, which is subdivided into n areas respectively encompassing an identical plurality of columns with simultaneous access to such areas (col. 1, line 66 – col. 2, line 1, Penzel).

Penzel teaches that the row address decoder 5, in accordance with the actual row address, selects one of the 512 rows of the memory field 12 (col. 3, lines 23-25, Penzel).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Keevill et al.'s patent with the teachings of Penzel by including an additional step of using an apparatus, wherein data positions in said buffering means are conceptually arranged in columns of data positions and rows of data positions, wherein said first register means and said second register means are for storing a column of data, and wherein said third register means is for storing a row of data. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to organize the stored data in different locations so that it will be easy to access particular data by row address or column address.

- As per claim 28, Keevill et al. and Penzel teach the additional limitations.

Penzel teaches an apparatus, wherein said first read/write means reads data from a column in said buffering means prior to when said second read/write means writes data to the same column in said buffering means (col. 7, lines 30-41, Penzel).

- As per claim 29, Keevill et al. and Penzel teach the additional limitations.

Penzel teaches an apparatus, wherein said third read/write means is activated each time all the data in said buffering means has been rewritten (col. 7, lines 30-41, Penzel).

9. Claim 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keevill et al. (US 6,359,938 B1) as applied to claim 26 above, and further in view of Wang (US 6,014,411).

As per claim 30, Keevill et al. substantially teach the claimed invention described in claim 26 (as rejected above).

However Keevill et al. do not explicitly teach the specific use of an apparatus, wherein said decoding means comprises an a posteriori probability decoder.

Wang in an analogous art teaches that the first APP decoder starts its backward recursion from the all-zero state with probability 1 (figure 7, col. 14, lines 44-46, Wang).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Keevill et al.'s patent with the teachings of Wang by including an additional step of using an apparatus, wherein said decoding means comprises an a posteriori probability decoder.
This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using an apparatus, wherein said decoding means comprises an a posteriori probability decoder would provide the opportunity to apply a-posteriori probability algorithm in both forward and backward recursions using soft metrics based on channel characteristics and a-posteriori probabilities of bits being zeros or ones.

- As per claim 31, Keevill et al. and Wang teach the additional limitations.

Wang teaches an apparatus, further comprising means for making a hard decision for each bit position of input data (col. 14, lines 48-49, Wang).

Specification

10. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

11. The pre-amendment of 10/21/2003 was entered.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 703-305-7853. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dipakkumar Gandhi
Patent Examiner

Guy J. LAMARRE
PRIMARY EXAMINER